Update on CSP Assembly Reliability and JPL-led MicrotypeBGA Consortium

by
Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology

ABSTRACT

Availability of board solder joint reliability information is critical to the wider implementation of Chip Scale Packages (CSPs). This paper will compare three different CSP concepts as well as their assembly reliability. In addition, literature cycling data on solder joint reliability of several numerous low I/O packages will be projected for a specific thermal cycling range using a modified Coffin-Manson relationship. A MicrotypeBGA consortium with industry-wide support was organized by the Jet Propulsion Laboratory to address technical issues regarding the interplay of package types, I/O counts, PWB (Printed Wiring Board) materials and types (standard and microvia), and manufacturing variables on quality and board reliability. The most current results from this program will also be presented.

WHY CHIP SCALE PACKAGES

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are now at the stage that Ball Grid Arrays (BGAs) were about two years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSP as the package that is a miniaturized version of the previous generation. Two concepts of CSPs are shown in Figure 1. The concepts presented include: (1) packages with flex or rigid interposer and (2) wafer level molding and assembly redistribution.

Packaging accomplishes many purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pad metallurgy for reflow assembly processes.
- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPs do not permit significant redistribution and the current cost effective PWB fabrication limits full adoption of the technology, especially for high I/O counts.
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation.
- Eases die functionality testing.

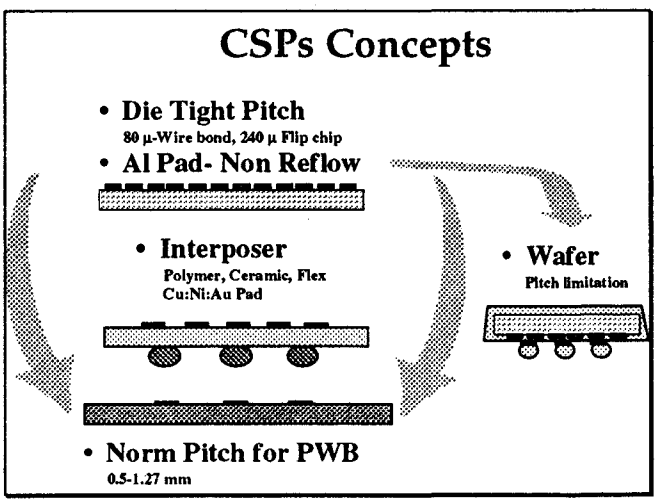


Figure 1: Two Chip Scale Package Concepts

SELF ALIGNMENT OF MICRO TYPE BGAS

CSPs can be categorized into grid arrays and leads (no leads) using the I/O expandability and manufacturing robustness as shown in Figure 2. Key advantages/disadvantages of each category are also listed. The mini (fine pitch) grid arrays can

accommodate higher pin counts, and similarly to BGAs, they have self alignment (centering) characteristics. For BGAs, the ease of package placement requirements has been widely published as one of their attributes. This attribute has permitted reduction in the number of solder joint defects to lower levels than conventional SM packages.

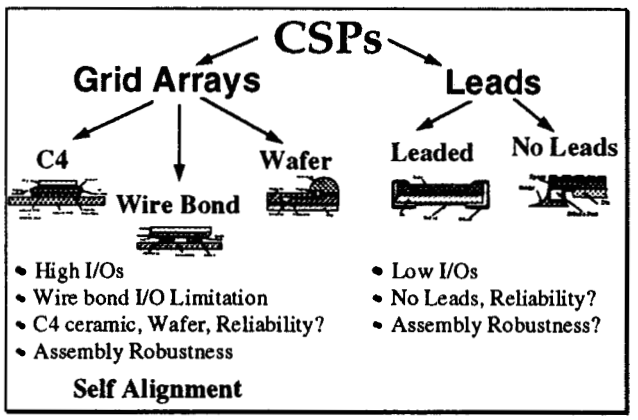


Figure 2: Two Chip Scale Package Categories

Many factors affect self alignment characteristics, but the main factor is the molten solder surface tension that provides the pull force on the package toward the pad centers. The counter force is the weight of the package. For Plastic BGAs (PBGAs), the pull forces induced from the melt of eutectic balls are larger than the forces from the partial molten joints in the ceramic BGAs (CBGAs) or solder paste melts in conventional packages. Hence, better self alignment for PBGAs. The symmetry of BGA ball patterns helps further in permitting both X and Y as well as rotational placement offsets for BGAs. For grid CSPs, the molten surface tensions are much smaller than BGAs since they have lower solder ball volumes. This, coupled with the CSPs finer pitch, can degrade their self alignment performance, especially with heavy packages. Therefore, the CSPs might require much tighter placement accuracy than the 50 mil pitch BGAs.

Grid CSPs show self alignment, but there is disagreement on what are the allowable offset limits. The acceptable placement offsets for variety of packages including grid CSP were quantified[1]. An offset of only 25% for a grid CSP with 46 I/Os was acceptable. The acceptable offsets were 62% for PBGAs and 50% for CBGAs. The CSP offset was reported to be 80% by another investigator[2]. It was also qualitatively determined[3] by hand placement of three hundred fifty CSP packages, reflowing, and counting the joint defects. It was reported that out of 16,100 solder joints, only two bridges were observed, which were determined to be due to the presence of foreign materials. No defects were found due to placement inaccuracy.

CSP ASSEMBLY RELIABILITY

The thermo-mechanical wear (creep) of solder joints is the cause of failure for most CSP board assemblies. Failure of a solder joint can be caused by mechanical stresses in a non-uniform thermal expansion and/or by contraction of different materials in the assembly. To achieve the least damage to solder joints, thermal mismatch between the die and board should be minimized either by package optimization or by appropriate board material selection to closely match coefficient of thermal expansion (CTE) of the package. Only a few of the CSP packages have been designed to alleviate damage due to the thermal expansion of package/board mismatches.

Table 1 categorizes assembly reliability of packages for three levels. It includes literature reliability experiment data for packages with flex or rigid interposers and wafer level packages. Reliability data for a few other packages from literature were reviewed previously[4]. Aspects of cycling conditions with their failure mechanisms are summarized in the following.

CTE Absorbed CSP

Thermal cycling test results for a CTE-mismatched relieved package are shown in the Table 1. This package uses TAB-like IC interconnects, a resilient elastomeric interposer, and eutectic solder balls. The resilient interposer in conjunction with the springiness of the TAB interconnection reduce thermal expansion differences between the chip (CTE 2-3 ppm/°C) and the PWB (CTE for FR-4 ~15 ppm/°C). This package has been shown to be reliable, robust, with no requirement for underfilling. Thermal cycling/shock data given in the Table were for daisy chain packages on FR-4 and were performed from the liquid nitrogen temperature (-196°C) to hot oil (160°C).

Because of the low strain state of solder joints, fatigue failure mechanisms of solder joints were not observed and failures shifted to the heel of TAB interconnection with high mismatched stress levels. Significant improvement was observed when ductile gold leads were used. The gold version showed no failure up to 2000 cycles in the range of -65°C to 150°C. The thermal cycling screening test results associated with assembly exposures to extremely low temperatures (stress conditions) and high temperatures (strain conditions) are not realistic and therefore their failure mechanisms may not be representative of field failures.

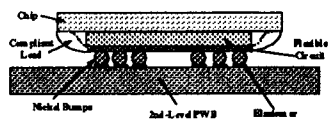
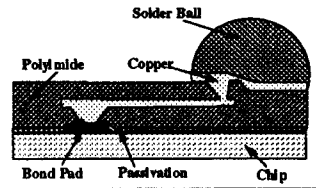
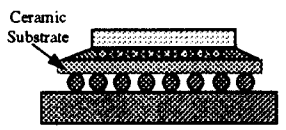
One such failure, due to extreme high temperature exposure, is the chambering and deformation of FR-4 close to its glass transition temperature (Tg). The PWB materials show severe damage if the cycling temperature becomes close to or exceeds their glass transition temperatures (the temperature that polymer materials start to become soft). Indeed, it was observed that FR-4 plated through holes had massive barrel cracking failure for the -65°C to 150°C temperature cycling range.

Extreme CTE Mismatch

Thermal cycling test results for assembly of a wafer redistributed package is shown in Table 1. In this package, a thin film metal/polymer redistributes the location of the solder bumps over the chip to make these compatible with the surface mount footprint. The height of the package type increases by the thickness of the metal polymer layer from the bare chip. This additional layer will not generally absorb the CTE mismatch between the chip and the board and therefore the assembly reliability of these package is expected to be very similar to Controlled Collapse Chip Connection (C4) assemblies.

Without the underfill materials, the assembled package failed in less than 40 cycles when subjected to thermal cycling between 0°C and 100°C. For these types of packages, underfilling is usually required to achieve an acceptable level of assembly reliability. The underfilled assemblies did not fail up to 2,000 cycles.

Table 1 Literature Data on CSP Assembly Reliability

Package Type Schematic (not to scale)	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References (comments)
Flex Interposer CTE matched 	-196°C<>160°C -65°C<>150°C	130 no underfill 1163 2000*	0/3 0/46 0/34	18 8 18 8	J. Fjelstad, T. DiStefano, B. Faraji, C. Mitchell, z. Kovac, "mBGA Packaging Technology for Integrated Circuits," *NEPCON East*, June 1995 T. DiStefano, J. Fjelstad, "Chip-scale Packaging meets future design needs," *Solid State Technology*," April 1996 * Gold bond ribbon. Ductile-copper bond ribbon survived 500 cycles.
Wafer Level Redistribution 	0°C <> 100°C (Thermal Shock)	>2000 underfill <40 no underfill	NA	26 6	R. Chanchani, et al, "mini Ball Gird Array (mBGA) Assembly on MCM-L Boards," *Proceedings of Electronic Components and Technology Conference*, May 18-21, 1997
Ceramic CSP 	-40°C <>125°C	~600* no underfill, PWB 0.6 mm >900* no underfill, PWB 1.6 mm	NA	22 0	R. Ianzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Technology," *Proceedings of second International Conference on Chip Scale Packaging, CHIPCON* '97, Feb. 20-21, 1997 *Private Communication

Ceramic Packages with Rigid Interposer

The non-wafer level ceramic packages have shown reasonable assembly reliability with no underfilling. Thermal cycling results for a ceramic package on FR-4 is also included in Table 1. The ceramic CSP uses the same design rules as multilayer ceramic (MLC) with the first level interconnection choices of thermal compression and gold stud bump, solder flip chip, and wire bond. The strength, rigidity, coplanarity, and

chamber of package are excellent. The package assembly on a 0.6 mm low Tg FR-4 failed at about 600 thermal cycles between -40°C to 125°C. Cycles to failure increased to more than 900 cycles when PWB thickness increased to 1.6 mm. Thicker FR-4 is expected to show better rigidity when exposed to 125°C, a temperature close to the low Tg FR-4 polymer used for this study.

CRITICALITY OF FAILURE MECHANISMS

Failure at the board level could also be caused by the internal failure of the package. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure shift from the solder joint to the internal package. This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies. This and other failure mechanisms which are being established for CSPs must be understood by a modeler before being able to predict a meaningful reliability projection. An example of a projection without consideration of failure mechanisms is shown in Figure 3. The cycles to failure projection based on solder predicts a life of more than 7,000 cycles for a thermal cycle profile of -55°C to 125°C. This is an order of magnitude larger than experimental cycles to failure of 1,000 to 1,500. In addition to those referenced in Table 1, another author specifically reported the TAB failure just before assembly failure being detected at 1,000 cycles[5].

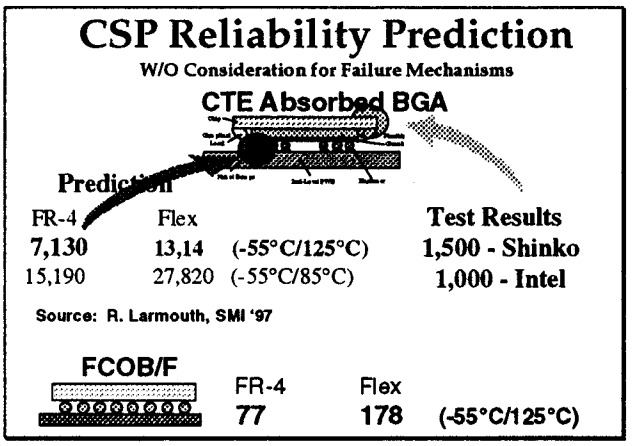


Figure 3 Fatigue Failure Projection based on the Wrong Failure Mechanism Assumption for a CTE Absorbed CSP.

BOARD RELIABILITY FOR SM PACKAGES AND THOSE PROJECTED FOR CSPS

Reliability of conventional SM packages have been investigated at JPL. Cycles to failure test data points and their Weibull distributions for 28-, and 20-pin LCC, and 68-pin gull wing assemblies are shown in Figure 4. Thermal cycling ranged from -55°C to 100°C with a 246 minute duration. The failure distribution percentiles were approximated using a median plotting position, $Fi = (i-0.3)/(n+0.4)$. The two-parameter Weibull cumulative failure distribution was used to fit the data.

For comparison, projected cycles to failure for low count CSPs are also included. Results are those gathered from literature and projected from a modified Coffin-Manson relationship. Board reliabilities of most CSP packages are comparable or better than their LCC counterparts. These packages, however, are not as robust as leaded packages including gull wing and J-leads. Data for J-leads are not shown in the Figure since there were no joint failures up to 3,000 cycles.

A SYSTEMATIC APPROACH TO ASSESS CSP BOARD RELIABILITY

Board reliability information is essential for CSP implementation for high reliability applications and to ease their use in commercial sectors. For wider application of this technology, the potential user will need design reliability data since they often have no resources, time, or ability to perform complex environmental characterizations. To help to build the infrastructure in these areas, JPL has formed a consortium with objectives of addressing many technical issues regarding the interplay of package types, I/O counts, PWB materials, surface finishes, and manufacturing variables for the quality and reliability of assembly packages.

The JPL-led Consortium Objectives and Accomplishments:

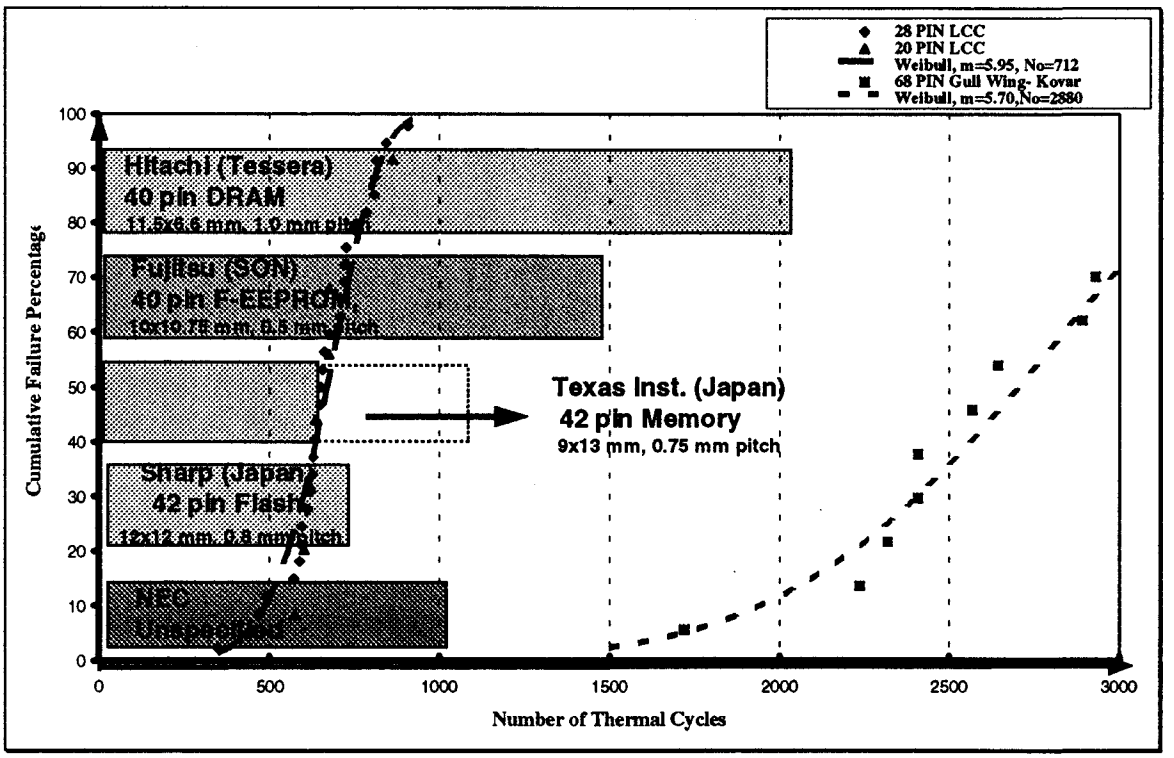
A consortium was formed from the team members of the original JPL-led BGA consortium[6] and new members added with experience in this technology. All participants have furnished in-kind contributions by providing their expertise and resources required to complete the objectives of the program. The wide industrial use of emerging chip size packages will afford NASA as well as consortium industries inexpensive access to this technology and support miniaturization thrusts for their next generation applications.

The objectives of the program are to demonstrate controls, quality, and reliability of CSP interconnects and to support the development of an industrial infrastructure for product assurance and inspection methodology development, especially for the assembly level. These include:

- Characterization of the optimal package type configuration
- Reliability characterization of package type, I/O, and environmental dependency
- Reworking techniques

Design of Experiment (DOE) methods were used to improve effectiveness. Variables which were toggled included: package I/O and configuration, PWB materials, manufacturing processes, and environmental conditions. Inspection techniques such as X-ray, C-SAM, and SEM will be used to determine damage progress during environmental exposure. Cycles to failure data will be analyzed using Weibull failure distributions and the Coffin-Manson relationship for life projections.

Diverse participants, including those from military and commercial sectors permitted implementation of the objectives of the program in a concurrent engineering environment.



*No failure of J-leads to 3,000 cycles

Figure 4. Projected Cycles to failures for Low Pin Count CSP Assemblies and Cumulative Failure Distributions for Conventional SM Package Assemblies Tested at JPL (-55°C to 100°C)

CHALLENGE OF CSP TECHNOLOGY IMPLEMENTATION

In the process of building the first test vehicle of CSPs, many challenges were identified regarding various aspects of technology implementation. Key challenges are summarized as follows:

Maturity and availability— Availability of CSPs for use and attachment reliability evaluation is the most challenging issue. There are numerous publications on a wide range of CSPs, but most packages are at their early stages of development and lack package reliability data. Assembly reliability data are rare. Most packages were available in prototype form and this does not guarantee the uniform package characteristics for the production version or even their availability. Delay on package delivery from the projected time is the norm.

Lack of Design Guideline Standards— Currently, guidelines and standards on various elements of CSPs are not available. For our design, guidelines developed by the package suppliers were used when available. Otherwise, available knowledge and engineering judgment were considered. Packages chosen had different pitches, solder ball volumes, solder ball compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes. Board design guidelines are needed, especially for the build up (microvia) configuration.

PWB Materials— The standard PWB design could be used for low I/O CSPs. Our test vehicle included several of these packages with the objective of characterizing assembly reliability when conventional PWB design was used. Higher I/O packages with active dies require the use of buildup (microvia) board technology. For testing purposes, however, it was possible to design high I/O daisy chain packages on a standard board. Another version of our test vehicle included a PWB with microvia technology.

Applications— There were a number of packages from low I/O (<50) to higher I/Os selected for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM packages, direct chip attachment, BGAs, and CSPs on one board is another expected design and assembly challenge.

Test Vehicle Design

The consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

Package— Numerous packages from leaded and leadless to micro type ball grid arrays selected for evaluation. I/Os ranged from 12 to 540 to meet the short and longer term applications.

PWB Materials and Build— Both FR-4 and BT (Bismaleimide Triazine) materials were available in the resin copper coated form for evaluation. Both standard and microvia board technologies were used. In design of daisy chains, it became apparent that the standard PWB technology could not be used for the majority of packages.

Surface finish— At least three types of surface finishes are being considered for evaluation: OSP, HASL, and Au/Ni. Other surface finishes are also being considered. Three types of solder pastes will be evaluated: no clean, water soluble and RMA.

Underfill— Packages with underfill requirements will be evaluated both with and without underfill to better understand the reliability consequence of not using underfill.

Test vehicle feature— The test vehicle is 4.5 by 4.5 inches and divided into four independent region. Each region has four daisy chains and can be cut for failure analysis without affecting the daisy chains of other regions. All packages are daisy chained and they have up to two internal chain patterns.

Environmental testing— At least three conditions are considered; -30 to 100°C and -55 to 125°C, to link our data to those generated for the Ball Grid Arrays. Also, thermal cycling will be performed between 0 and 100°C to meet the needs of commercial team members. In addition, mechanical vibration and shock will be performed and theoretical modeling will be carried out as needed.

Status of the MicrotypeBGA Program

The consortium has completed the design of two test vehicles: one from collective team effort (TV-1) and the other initiated internally by a team member (TV-H). The trial assembly of the TV-H is now complete. These assemblies are currently being evaluated to determine if changes are required prior to the production. The only challenge remained is the process optimization for a flip chip package. Flip chips with and without bridges were built. One possible reason for bridging is the lack of solder masks between the pads which was not feasible to apply because of the fine pitch pattern.

The TV-1 trial boards were built to optimize the assembly processes and to verify continuity of daisy chains. The consortium is currently assembling the trial test vehicles using sixteen packages from nine suppliers. I/Os are from 12 to 540. Full production will be followed after all aspects of the test vehicle were verified for compliance to design.

CONCLUSIONS

- Self alignment which translates to ease of package placement onto the board is a key attribute of grid CSPs compare to the leaded version. The offset

placement levels which result in acceptable solder joints are not well established. It was postulated that a tighter placement control might be required for CSPs, than those reported for BGAs.

- CSP assembly reliability depends on the types of package, the lowest values for wafer level, medium for ceramic, and highest for the CTE absorbed categories. Underfill is required for wafer level packaged; it could also be used to enhance reliabilities of most other packages.

- The projected thermal cycles to failure of solder joints for several low I/O CSP packages were lower than the test results of surface mount leaded packages performed at JPL. These package had comparable or better reliabilities than the low I/O leadless packages.

- Traditionally, solder joint failure was considered to be the weakest link in the microelectronics attachment reliability. This might not be true for CSPs with an innovative design. It was shown that projection by a modeler based on solder joint failure was an order of magnitude higher than experimental test results.

- Cycling temperature range in some cases might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analyses need to be performed to build confidence in assembly reliability results.

The JPL-led consortium was formed to systematically address many of the CSP assembly reliability issues. Understanding of the overall philosophy of testing to meet system requirements, as well as detecting new failure mechanisms associated with these miniaturized packages, are key in collecting meaningful test results and building an infrastructure for this technology.

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